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IMPLEMENTATION ON CLOCK GENERATION OF 25MHZ USING TRANSLATION BUFFER INTERFACE FROM ECL-CMOS

Rekha Murthy & Amulya H.G

Assistant Professor, Department of Electrical & Electronics, SVIT, Bangalore, India

ABSTRACT

The propitious crystal oscillator is considered as utmost important in a high speed application, since it can dispense the clock reference for the entire clock distribution system. In the proposed paper, a circuit principle is presented to realize an extremely fast ECL to CMOS logic conversion, where the possibility of generating clock frequency of 25MHz is obtained instead of a crystal oscillator. SPICE is found as a mixed use circuit analyzer that simulates electronic circuits and can perform various analysis on electronic circuits. By employing PSPICE, the analysis of the circuit has been proffered in this paper. Also, this paper describes about the significance of crystal oscillator which can be designed using emergent technology described for high speed application.

KEYWORDS: *Crystal Oscillator, Clock Frequency, ECL to CMOS Logic Converter, PSPICE Software*

Article History

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INTRODUCTION

Crystal oscillators were feigned in the 1920s. Cady found one of the first ones in 1921. Miller patented both his own and Pierce's circuits in 1930 [l]. Pierce patented both the own and Miller's circuits in 1931 [2], and after some legal arguing in the courts, Pierce reattempted both circuits again in 1938 [3]. Sabaroff's quartz crystal version of the Colpitts LC oscillator was published in 1937 [4], and Meacham's resistance bridge loop was published in 1938. Butler published the article on VHF harmonic oscillators in 1946 [6]. Goldberg and Crosby published their article on cathode coupled or grounded grid oscillators in 1948 [7]. The U.S. Army Signal Corps funded an intense quartz crystal development program during and after World War II and funded a small amount of oscillator circuit development along the way. Edson did a study of VHF harmonic oscillator circuits in 1950 and published his classic book on vacuum tube oscillators of all types in 1953. In 1965, First published the design handbook [l0] on the Pierce circuit and the Butler common base harmonic circuit. The early oscillators utilized vacuum tubes, which had a limited life and were, therefore, high-maintenance items. Consequently, there was a substantial advantage in using a one-tube oscillator circuit, as compared with a two-tube circuit. The strong demand was placed on getting the maximum power out of the oscillator circuit, since this meant that fewer power amplifier tubes were required in a transmitter. Vacuum tubes are operated at power supply voltages of 150-300 V DC, which allows large voltage quivers and made it extremely easy to overdrive the crystal's dissipation limit or even fracture the crystal. With the dawn of transistor and IC circuits, the emphasis was placed on performance. Transistors are very small and have indefinite life, so in many cases, the number of transistors employed

in an oscillator circuit are all most irrelevant. The power supply voltage used in transistor circuits has reduced the crystal exploit the problem to more manageable proportions. And to get better frequency stability, oscillator circuits are now routinely designed with low power output, with the effect of an addition of an amplifier stage it reduces the cost.

ECL does not produce a large voltage swing between the LOW and HIGH levels. Instead, it has a small voltage swing and it internally switches current between two possible routes, depending on the output state. The first ECL logic family was introduced by General Electric in 1961. The concept was later refined by Motorola and others to produce the still popular 10K and 100K ECL families. These groups of devices are extremely fast, offering propagation delays as short as 1 ns. The newest ECL family, ECL in PS (literally, ECL in picoseconds), offers maximum delays under 0.5ns (500 ps), including the signal delay getting on and off of the IC package. Throughout the evolution of digital circuit technology, some type of ECL has always the fastest technology for discrete, packaged logic components. Still, commercial ECL families are not nearly as popular as CMOS and TTL, mainly because they consume much more power. In fact, high power consumption made the design of ECL supercomputers, such as the Cray-1 and Cray-2, as much of a challenge in cooling technology as in digital design. Also, ECL has a poor speed-power product, does not provide a high level of integration, has fast edge rates necessitate design for transmission-line effects in most applications, and is not directly compatible with TTL and CMOS. Nevertheless, ECL still finds its place as a logic and interface technology in very high-speed communications gear, including fiber-optic transceiver interfaces for gigabit Ethernet and Asynchronous Transfer Mode (ATM) networks.

PROBLEM DEFINITION

To understand the technological improvements, one must remember that the CPU is a data processing gadget, mounted on a printed circuit board (the motherboard) .Most of the data processing takes place inside the CPU. However all data must be transferred to and from the CPU via the system bus. The speed of the CPU can be determined by the speed of the crystal oscillator which is nothing but the clock frequency.

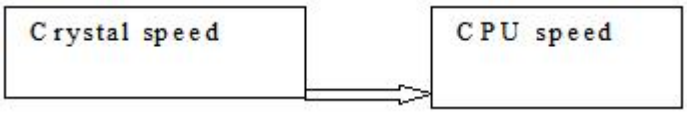

Figure 1: Block Diagram

From the block diagram the crystal on the motherboard which continually ticks to the CPU at a substantial number of clock beats per second. At each clock tick something happens in the CPU. Thus, the more ticks per second –the in addition data are processed per second.

The first CPUs worked at a frequency of 4.77MHz.Then the clock frequencies rates rose to 16, 25,50,66,90,133 and 200MHz.Clock frequencies are still being increased. In a few years CPUs will be operating at 3GHz and more. To reach these high frequencies, one has to utilize an approach called clock doubling.

Intel's 80486DX2 25/50MHz was pioneer chip with clock doubling .If the motherboard crystal works at 25MHz, the CPU will receive a signal every 40 nano seconds(ns).Internally in the CPU ,this frequency is doubled to 50MHz. Now the clock ticks every 20ns inside the CPU. This frequency supervise all internal transactions, including integer unit, floating point unit with all memory management unit operations on the side others. The only area still working at 25MHz are external data transfers to RAM, BIOS and the I/O ports.[11]

Due to this reason to improve the performance of CPU instead of using crystal oscillator designed using op-amp or BJT the circuit has been implemented using the equivalent high speed ECL-CMOS converter which capable of generating 25MHz clock frequency. This designed circuit can be applicable for Intel's 80486DX2 25/50MHz to improve for high speed data transmission.

SPECIFICATIONS AND TYPES OF ECL

Emitter Coupled Logic (ECL), sometimes concerned as Current Mode Logic, which is an extremely high-speed digital technology. ECL has a propagation time of 0.5 to 2 ns, which is much faster than TTL and power dissipation 3 to 10 times higher than that of TTL.

The outset logic of ECL, much like that of TTL, fluctuates from a ground-level to a HIGH state. However, the voltage levels of these states deviate from ECL and TTL.

The output logic swing of ECL gates varies from a LOW state of -1.75 volts to a HIGH state of -0.9 volts with reference to ground. The following table is an illustration when positive logic is used when referred to logic "0" or "1".

Table 1

Voltage Level	State	Logic	Boolean
-1.75V	LOW	False	0
-0.9V	HIGH	True	1

There are normally two supply voltages specified. The more positive supply voltage is labeled V_{CC} and the more negative supply voltage V_{EE}. Usually, only one supply voltage is used, and the other is ground. ECL evaluation boards with both positive and negative voltages are used in order to simplify interfacing with ground-referenced instruments.

In the new ECLinPS and ECLinPS Lite families of GHz ECL devices, both 10 K and 100 K devices can share the same supply voltages of V_{CC}-V_{EE} = -5.2 V. The industrial standard for ECL supply voltages are V_{CC}=0 V, and V_{EE} = -5.2 V.

LVECL devices are ECL devices designed for use with V_{EE} = -3.3 V. They are I/O compatible with standard ECL devices.

The "P" in PECL stands for positive. PECL Circuits are generally identical to ECL circuits, except the V_{CC} supply is 5 V and the V_{EE} supply is ground. There are different types of PECL devices that are accomplished strictly for +5 V supply only.

LVPECL Circuits are PECL circuits performs with V_{CC} = 3 V or 3.3 V, the same supply voltage as for Low Voltage CMOS devices. The PECL and LVPECL devices are designed to be supply voltage adaptable with TTL/CMOS and LVCMOS circuits, respectively.[5]

INTERCONNECT INDUCTANCE

Interconnect wiring must be considered, when creating any high-speed electrical circuit. At low frequencies the effect of interconnects is negligible, but with today's higher frequencies, designers must think about the interconnects effect on persuance.

Interconnect is the conductive path required to achieve connection from one circuit element to the other part of the circuit. Current flowing through conductors create magnetic fields (Ampere's law), which when varying with time create induced electric fields (Faraday's law). These induced electric fields exert forces upon the electrons in the conductors and cause a drop in the electric potential. This is what causes the parasitic inductance that influences a circuit's performance. The material properties of the wiring such as the dielectric constant, resistivity, propagation medium, and permeability have to be taken into account.

If the interconnect line is long, a large inductance occurs if the rise times get faster and L dI/dt grows. Then the transmission line effects surface, and both the inductance and capacitance must be taken into account. Because of the inductance, the current line cannot be increased indefinitely by decreasing source resistance of a driver. The inductors resist fast changes in current by procreating a reverse electromotive force. This confines the amount of current flowing through a line and restricts how fast voltage/current waveform can travel. A limited current can charge up only a certain length of a capacitive line at a given time. When designing a circuit it is difficult to protend exactly how parasitic resistance, capacitance and inductance will alter the desired outcome. Modeling and simulation are key tools for presuming the operating characteristics of electronic circuits before they are built.

SIMULATION RESULTS AND DICUSSIONS

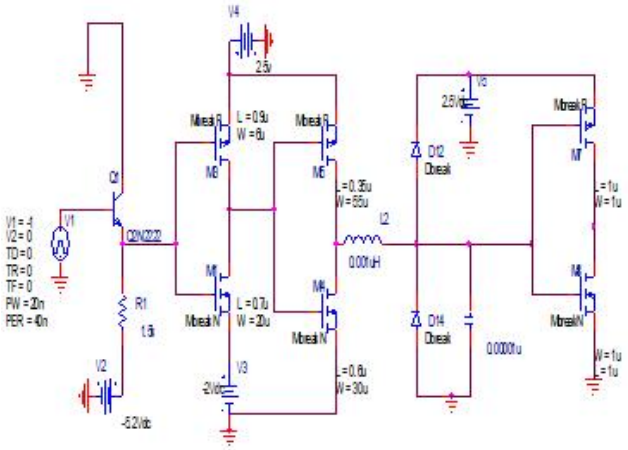

Figure 2: Circuit Diagram

Among many different values of positive rail, negative rail, and width and lengths for all 4 FETS. Finally settled on using the CMOS 2.5V positive rail, and initiating a new -2.0V negative rail. These particular connections to the voltage sources developed from the optimization of the circuit while experimenting with the W/L ratios of the transistors. The hardest part was trying to find the smallest values for W and L while still sustaining rise and fall times below 2 ns at node 11. For larger W/L ratios were necessary to charge and discharge the internal capacitance of the transistors invader to keep the rise and fall times below the minimum of 2ns. Then lowered the ratios as low as possible for the smallest area while still maintaining the required speeds. Finally settled with MP2 having a ratio of 55/.35 and MN2 with ratio 30/.6. After refining these ratios, the first CMOS ratios were adjusted in order to balance the system, settling on a ratio for MP1 of 6/.9 and MN1 of 20/.7.

The first stage of the circuit consists of emitter coupled logic which generates input square pulse of -0.674V to -1.667V. The output of this stage becomes as an input for the next stage which is nothing but buffer. The output node of this stage produces square pulse of 0V to 2.4118V.

The output of the buffer stage is connected to CMOS inverter through inductance acts as an interconnect as shown in figure 3.

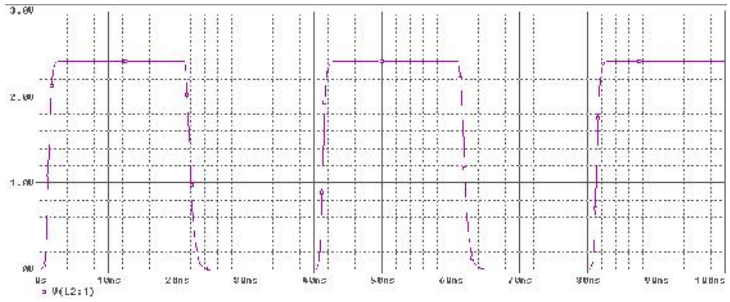

Figure 3: Output Waveform before Interconnect

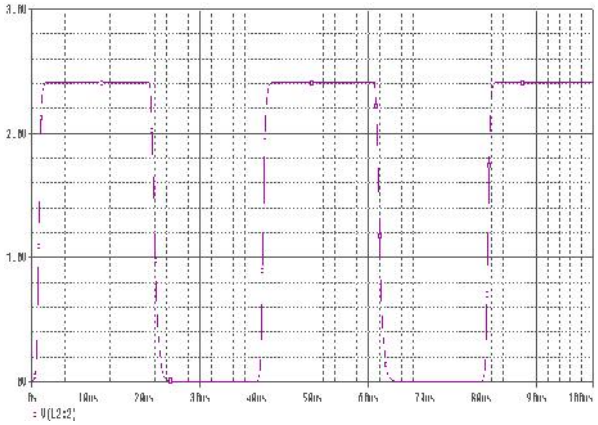

Figure 4: Output Waveform after Interconnect

With the input oscillation traveling at least 25MHz, the parasitic inductance resisted the fast change in current flow causing the waveform at node 11 to have bumps. The inductor inserted after the buffer and before the load CMOS gate made up for the interconnect inductance. The graph of the waveforms of the output of the buffer at node 11 and after the inductor at node 12 demonstrate how this circuit accounted for the interconnect problem.

The output of the interconnect is connected to CMOS inverter which provides the generation of 25MHz clock frequency as shown in figure 5.

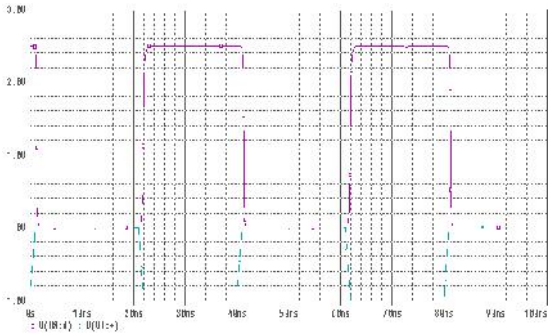

Figure 5: Output of CMOS Inverter

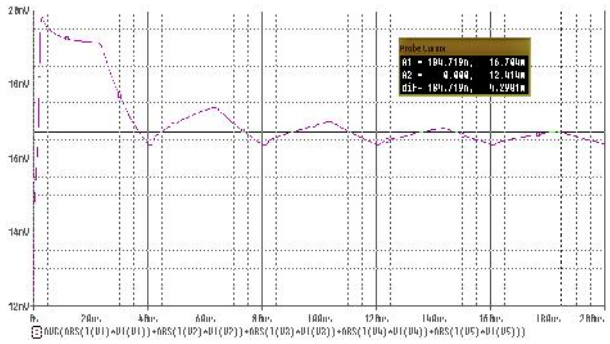

Figure 6: Power Dissipation at 25MHz

The minor changes to the W/L ratios of the second CMOS inverter can greatly affect the crest frequency of operation, with only a slight increase in the Figure of Merit.

Calculations

Area:

AreaMP1 = (6µm)(0.9 µm) = 5.4 μm^2

AreaMN1 = (20 µm)(0.7 µm) = 14μm^2

AreaMP2 = (55 µm)(0.35 µm) = 19.25μm^2

AreaMN2 = (30µm)(0.6µm) = 18μm^2

ATOTAL = 56.65μm^2

Power:

The power was averaged over 20 periods of operation at 25MHz and is as shown in the graph above.

Power = 16.704mW.

Propagation Delay:

tp = [(tPLH) + (tPHL)] * 0.5

= [(1.21ns) + (0.635ns)] * 0.5

= 0.92ns

Figure of Merit

FOM = Delay [ns] * Power [mW] * Area [µm2]

= 0.92 ns *16.704mW * 56.65μm^2

= 871

RESULTS SUMMARY

Table 2

Area(μm^2)	56.65
Power dissipation(mW)	16.704
Propagation Delay(ns)	0.92
FOM	871

CONCLUSIONS AND FUTURE ASPECTS

The application of an extremely fast ECL to CMOS logic conversion for generating clock frequency of 25MHz has obtained instead of crystal oscillator which makes the operation much faster that has been obtained with certain parameters as shown in the table.

The same result can be obtained for the generation of higher frequencies and can be further compared to the other emerging technologies that will exist in the system.

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